WHAT IS CLAIMED IS:

1. An apparatus comprising:

a line side circuit; and

a system side circuit to couple to the line side circuit via an isolation interface;

the system side circuit including:

a first clock signal generator to supply a first clock signal to the line side circuit via the isolation interface; and

a second clock signal generator to supply a second clock signal to the line side circuit via the isolation interface;

wherein the first and second clock signals when added sum to a signal having a substantially constant voltage.

2. The apparatus of claim 1, wherein the second clock signal is out of phase with the first clock signal.

3. The apparatus of claim 2, wherein each of the first and second clock signals has a substantially 50% duty cycle, and the first and second clock signals are substantially 180° out of phase with each other.

4. The apparatus of claim 1, wherein the first clock signal has substantially less than a 50% duty cycle and the second clock signal has substantially more than a 50% duty cycle.

5. The apparatus of claim 1, further comprising:

a first capacitor to couple the first clock signal to the line side circuit; and

a second capacitor to couple the second clock signal to the line side circuit.

6. The apparatus of claim 5, wherein the line side circuit includes:

a line side power supply;

a first diode to couple between the first capacitor and the line side power supply; and

a second diode to couple between the second capacitor and the line side power supply.

7. The apparatus of claim 6, wherein the line side power supply includes a third capacitor.

8. The apparatus of claim 7, wherein the line side circuit includes line monitoring circuitry to monitor at least one condition of a telephone subscriber line.

9. A chip set comprising:

a first integrated circuit (IC); and

a second IC;

the second IC including a first clock signal generator to supply a first clock signal to the first IC and a second clock signal generator to supply a second clock signal to the first IC;

the first IC including a first clock receive line to receive the first clock signal and a second clock receive line to receive the second clock signal;

wherein the first and second clock signals when added sum to a signal having a substantially constant voltage.

10. The chip set of claim 9, wherein the second clock signal is out of phase with the first clock signal.

11. The chip set of claim 10, wherein each of the first and second clock signals has a substantially 50% duty cycle, and the first and second clock signals are substantially 180° out of phase with each other.

12. The chip set of claim 9, wherein the first clock signal has substantially less than a 50% duty cycle and the second clock signal has substantially more than a 50% duty cycle.

13. The chip set of claim 9, wherein the first IC further includes:

a first diode to couple the first clock receive line to a power supply of the first IC; and

a second diode to couple the second clock receive line to the power supply of the first IC.

14. The chip set of claim 13, wherein the first IC includes line monitoring circuitry to monitor at least one condition of a telephone subscriber line.

15. A method comprising:

supplying a first clock signal from a system side circuit to a line side circuit via an isolation interface; and

supplying a second clock signal from the system side circuit to the line side circuit via the isolation interface;

wherein the first and second clock signals when added sum to a signal having a substantially constant voltage.

16. The method of claim 15, further comprising:

combining the first and second clock signals at the line side circuit to produce a substantially constant power signal for the line side circuit.

17. The method of claim 16, wherein the second clock signal is out of phase with the first clock signal.

18. The method of claim 15, wherein:

the first clock signal is supplied to the line side circuit via a first capacitor; and

the second clock signal is supplied to the line side circuit via a second capacitor.

19. A system comprising:

a line interface to couple to a telephone subscriber line;

a first circuit coupled to the line interface; and

a second circuit that is coupled to the first circuit via an isolation interface;

the second circuit including:

a first clock signal generator to supply a first clock signal to the first circuit via the isolation interface; and

a second clock signal generator to supply a second clock signal to the first circuit via the isolation interface;

wherein the first and second clock signals when added sum to a signal having a substantially constant voltage.

20. The system of claim 19, wherein the second clock signal is out of phase with the first clock signal.

21. The system of claim 20, wherein each of the first and second clock signals has a substantially 50% duty cycle, and the first and second clock signals are substantially 180° out of phase with each other.

22. The system of claim 19, wherein the first clock signal has substantially less than a 50% duty cycle and the second clock signal has substantially more than a 50% duty cycle.

23. The system of claim 19, further comprising:

a first capacitor to couple the first clock signal to the first circuit; and

a second capacitor to couple the second clock signal to the first circuit.

24. The system of claim 23, wherein the first circuit includes:

a power supply;

a first diode coupled between the first capacitor and the power supply; and

a second diode coupled between the second capacitor and the power supply.

25. The system of claim 24, wherein the power supply includes a third capacitor.

26. The system of claim 25, wherein the first circuit includes line monitoring circuitry to monitor at least one condition of a telephone subscriber line.